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Resolution of Damaged Metallization on Highly Complex Semiconductor Device

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Authors' contributions

This work was carried out in collaboration between both authors. Both authors read, reviewed, and approved the final manuscript.

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ABSTRACT

The paper focused on the resolution of damaged metallization during assembly process that lead to gross open-short (O/S) rejections during functional testing of a highly complex semiconductor package. Numerous batches were put on hold due to not meeting the specification assigned for the short contact test. Design of experiments (DOE) on assembly processes were conducted and eventually identified the reject as an electrostatic discharge (ESD) related failure. Corrective actions and ESD controls significantly reduced the occurrence of damaged metallization with around 85% reduction.

Keywords: Metallization; semiconductor; ESD; assembly.

1. INTRODUCTION

A common direction and most important objective of semiconductor manufacturing companies is to increase the production yields and maintain high quality while minimizing the wastage and assembly rejections. With new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are inevitable [1-4]. Short test failure provides significant rejects that substantially affects the final test yield and production delivery of a highly complex semiconductor device (Device Z). Majority of the

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process batches were put on-hold due to not meeting the 2% final test disposition criteria. Batches having test rejects > 2% were noticed on a span of several weeks as illustrated in Fig. 1.

2. EXPERIMENTAL SECTION

Analysis of test failure revealed that the major contributor to the rejection is the damaged metallization of the silicon die. Fig. 2 shows the investigation of test reject samples.

It was also noticed that a gold deposit was present along the location of damaged metallization. Cross-sectional analysis on the identified area revealed that an internal damage was seen on the passivation of the die. Two instances were normally observed when damaged metallization is seen on the passivation: 1) Gold deposition on the location of damage metallization; 2) Shorting of two metal layers which is only seen during cross-section of reject sample.

A complete process flow is given in Fig. 3, starting from silicon die fab going to pre-assembly (PA) until final test. Important to note that generally, process flow varies with the product and the technology [5-8]. Results of design of experiments (DOE) regarding process mapping show that damaged metallization would most likely to occur on pre-assembly and bumping station. This was identified after sending DOE failing parts for further failure analysis.

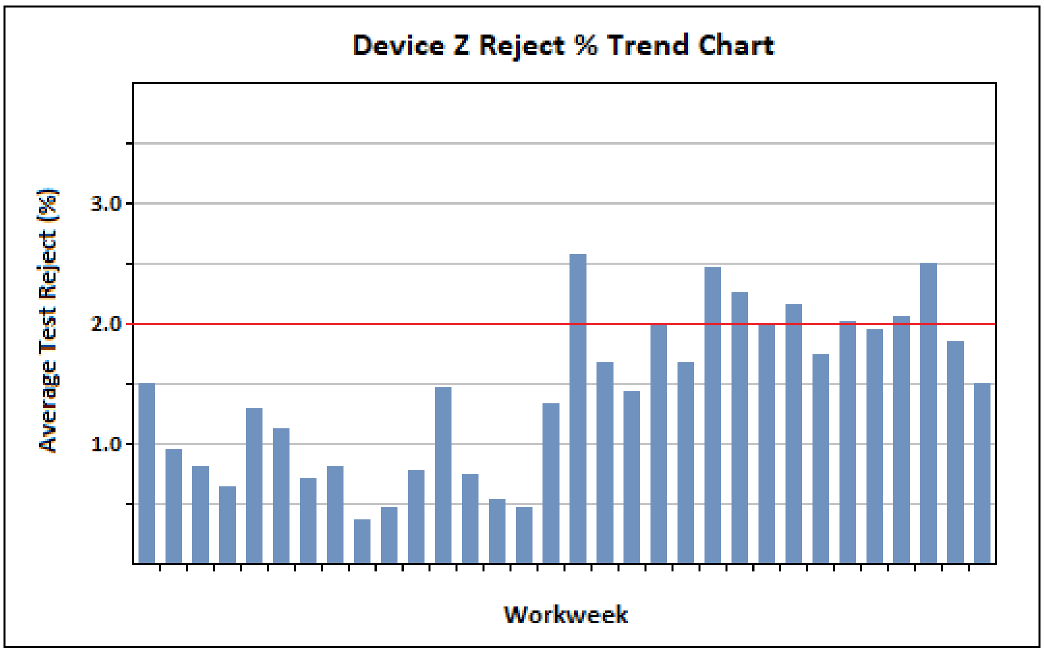

Fig. 1. Test reject percentage weekly performance

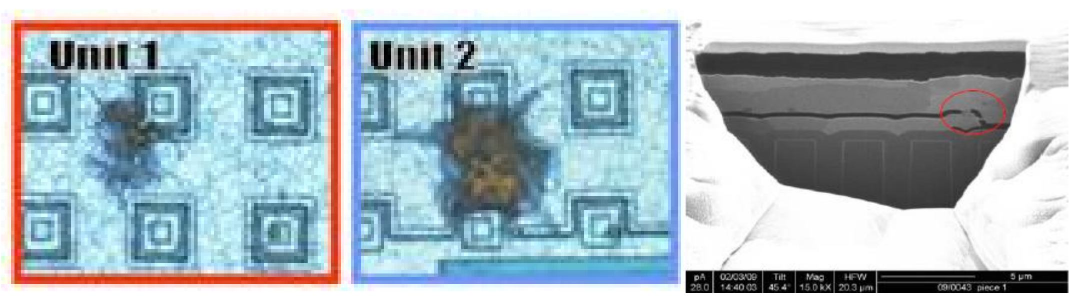

Fig. 2. Damaged metallization manifestation

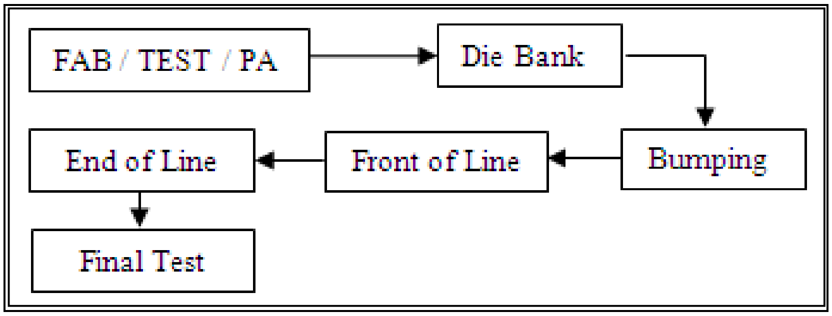

Fig. 3. Process macro map

Investigation revealed that gold deposits were present along the damaged metallization and the potential process that may cause the problem is the bumping process. Special remark is that bumping station uses gold deposition on its process.

3. METHODOLOGY

Cross-functional team was created, and brainstorming was made. A fault tree diagram was established as shared in Fig. 4. Several factors were identified and appeared as potential causes but only three scenarios were considered as the most probable, critical, and significant based on the signature of damage metallization.

Further brainstorming and process elimination narrowed down the variables that might cause damaged metallization. The three items identified are the following:

1. Machine-to-machine variation (specification and condition)
2. Device sensitivity on ionizer location (electrostatic discharge (ESD) phenomenon)
3. Limitation of inspection criteria

4. RESULTS AND ANALYSIS

Further analyses were employed on the three variables critically identified as potential causes of damaged metallization reject.

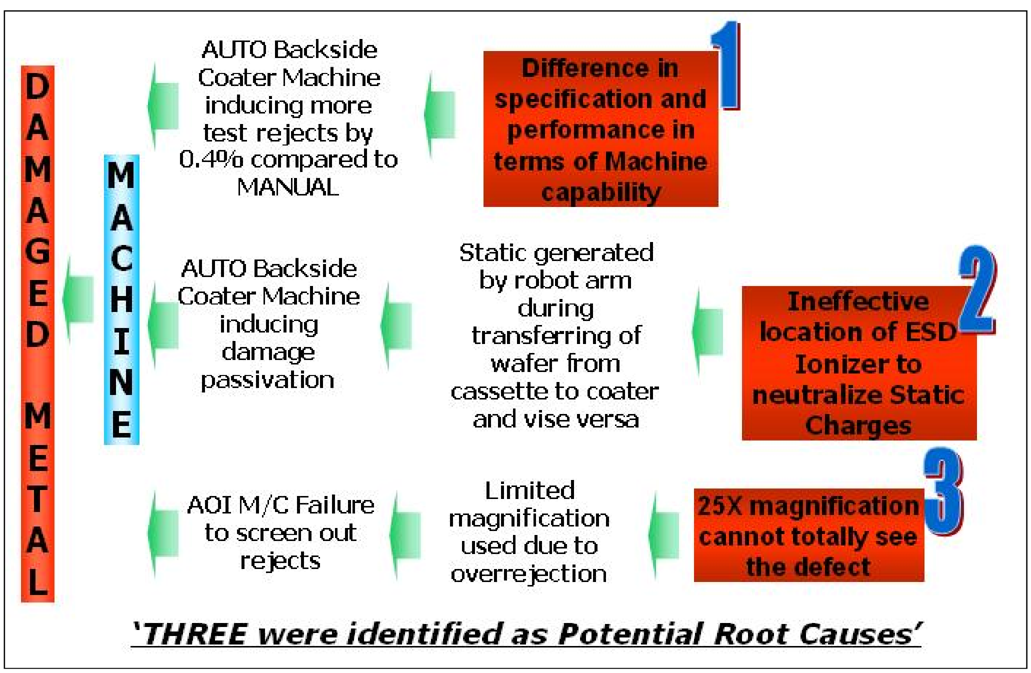

Fig. 4. Fault tree diagram

4.1 Machine-to-Machine Validation

Important findings included an observation of increased test rejects after backside coating for both manual and auto machines. Significant increase of test rejects was noted when auto backside was used as compared to manual backside coating.

4.2 ESD-Related Due to Ineffective Location of Ionizer

ESD was identified as one potential cause for damaged metallization that resulted to test reject. The damage manifestation seemed to be induced by ESD due to explosion effect on the part of the damaged metal as previously shown in Fig. 2. With this, ESD controls were checked particularly the ionizer setup as improved in Fig. 5.

Spin coating has the highest level of ESD. Measured field voltage level is around 380V which is much higher to the specification requirement of < 100V. Field voltage was measured using ESD event detector. The level of ESD measured was high, due to ineffective location of ionizer to neutralize the event. Discussion on the fundamentals of ESD and ESD damage could be found in the ESD Association references [9].

4.3 Limitation of Inspection Criteria

The current process flow did not have screening to discriminating the damaged metallization. And so automatic optical inspection (AOI) plus low magnification inspection was introduced. The new inspection criteria is given in Table 1.

4.4 Test Reject Monitoring

Significant effect was achieved in the average test reject per workweek performance after implementation of all improvement and corrective actions. Fig. 6 highlighted around 85% improvement in the test reject reduction caused by damaged metallization. Final test yield trend eventually stabilized after implementation of the identified corrective actions.

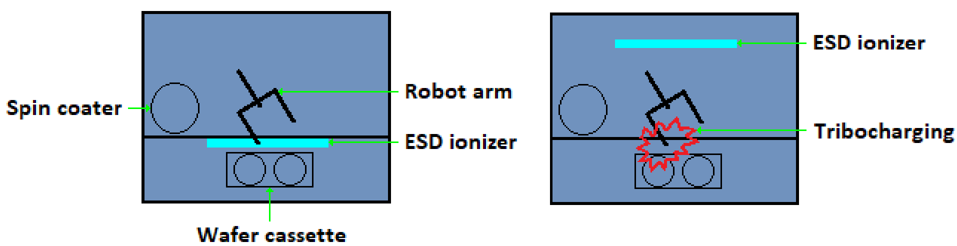

Fig. 5. Before vs after relocation of ionizer

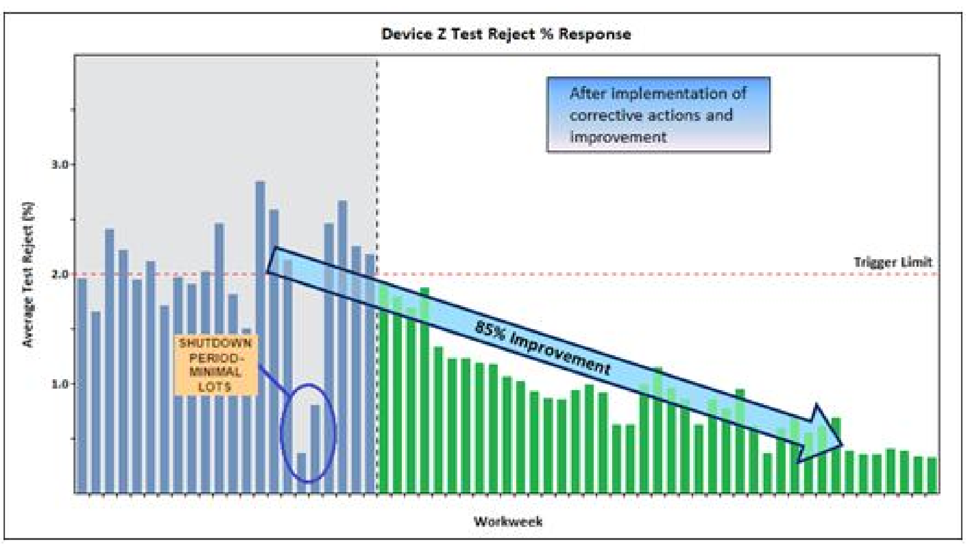

Fig. 6. Test reject performance improvement

Table 1. Inspection Criteria

Mode	Parameters
Complete Inspection	AOI 50x + Verification of AOI reject at High magnification (Hi-mag) + 100% Hi-mag inspection
Manual Inspection	100% Hi-mag inspection

5. CONCLUSION AND RECOMMENDATIONS

Different techniques for solving the damaged metallization were presented on this paper. Using the knowledge and understanding on data and circuit analysis lead us to pinpoint the phenomenon that caused the damaged metallization on a highly complex semiconductor package. DOE identified that the test reject is an ESD-related failure which was induced by the assembly process specifically the backside coating of bumping station. Relocating the position of ionizer significantly reduced the occurrence of damaged with around 85% improvement. Effectiveness of the corrective action was confirmed by the continuous reduction of test reject and the increase in the final test yield. Ultimately, damaged metallization was solved without too much cost involved and no major modification on the assembly process.

The learnings in this work could be used in other devices with similar situation and configuration. Comparison of existing works should also be included for added analysis. Worthy to note that continuous process improvement is really important to sustain the high quality performance of semiconductor products and their assembly manufacturing. As we were able to dig into the problem step-by-step, identified and validated the true causes, attained significant improvement, and recommended a permanent fix to the production line without cost involved and just by using available resources, implementation should carry on but with consideration to productivity point of view as using manual backside coating machine will give constraint to capacity. Studies and learnings shared in [10-12] are helpful in improving the assembly processes particularly in the yield improvement. It is also important that assembly processes observe proper ESD checks and controls. Studies shared in [9,12] are very helpful to realize proper and effective ESD-related controls.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
2. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. Proceedings of the 4th International Symposium on Electronic Materials and Packaging. Taiwan. 2002; 1-6.
3. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008; 1-11.
4. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
5. Geng H. Semiconductor manufacturing handbook. 2nd Ed., McGraw-Hill Education, USA; 2017.

6. Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA; March, 2016.
7. Harper C. Electronic packaging and interconnection handbook. 4th Ed., McGraw-Hill Education, USA; 2004.
8. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st Ed., Wiley-IEEE Press, USA; 2006.
9. ESD Association. Fundamentals of esd, device sensitivity and testing. USA; 2011.
10. Sumagpang Jr. A, Gomez FR. A methodical approach in critical processes optimization of new scalable package semiconductor device for ESD applications. Asian Journal of Engineering and Technology. 2018;6(6):78-87.
11. Pulido J, Gomez FR, Graycochea Jr. E. Lead scratch resolution through wirebonding process optimization on qfn packages. Journal of Engineering Research and Reports. 2020;15(1):29-33.
12. Gomez FR, Mangaoang Jr. T. Elimination of esd events and optimizing waterjet deflash process for reduction of leakage current failures on qfn-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018; 6(4):238-243.

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