



Semiconductor Package Design Solution for Addressing High-Density Configuration

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

The direction for integrated circuit (IC) packaging is getting smaller yet with increasing unit performance. In this case substrate-based technology became limited to miniaturization and downsizing direction. In this paper, a specialized design of IC is presented and discussed through augmentation of routing channels at the backside of the silicon die to eliminate the substrate application in the package. Routed channels are fabricated using plating or immersion process that are electrically connected to the bonding pads through conductive via within the silicon material. By eliminating the substrate re-distribution layers (RDL), a package is expected to decrease by 20 – 40% from its designed dimension.

Keywords: Substrate; BGA; semiconductor; assembly.

1. INTRODUCTION

A Ball Grid Array (commonly referred as BGA) is a type of surface mount technology (SMT)

packaging capable of more interconnections than other SMT devices like Quad-Flat No-lead (QFN) and Land Grid Array (LGA). A BGA is differentiated from the other packaging

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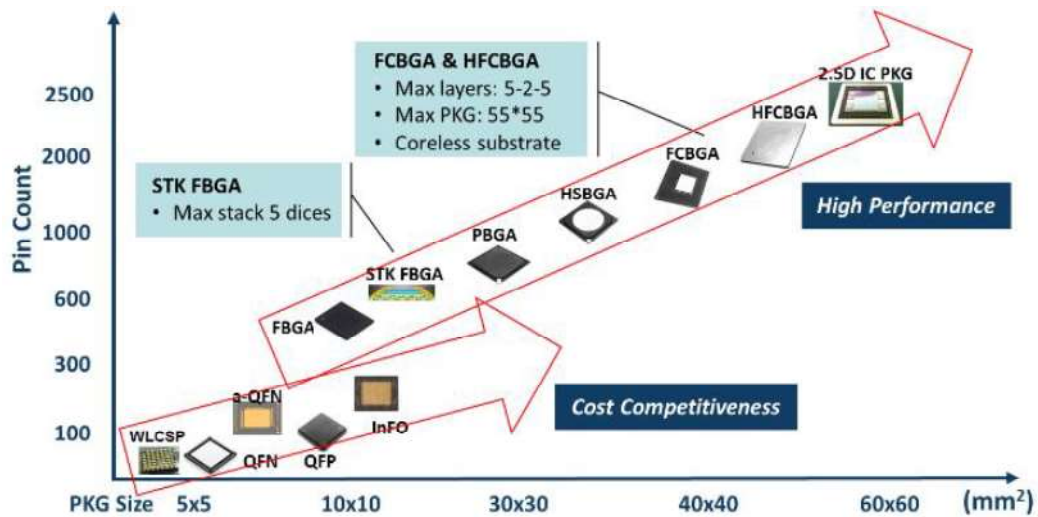


Fig. 1. Pin count and package dimension trend

techniques through the bottom contact pad, which is composed of solder balls that are electrically connected to the substrate, rather than exposed pad for QFN and LGA. Through this structural design, A BGA can cater input-output (I/O) capability of more than 150 bottom interconnections from the die bonding pads and substrate metal layers.

The direction to attain a downsized and miniaturized version yet moving to a higher performance of BGA device is a major detractor in packaging. As the pin count of a BGA device increases, the package dimension is also increasing at the same time creating a larger footprint for the device as illustrated in Fig. 1. Worthy to note that with new and continuous technology trends and breakthroughs, challenges in assembly manufacturing are inevitable [1-4].

The main reason for the increase of footprint is due to the additional re-distribution layers (RDL) layer that connect the solder balls to the bonding pad of the die. Usually, each solder ball is connected to a metal trace that is routed inside the substrate thru Via and channels that ends to a lead finger where it is bonded with a wire from the bonding pad. Normally, it is the size and area of the routing that dictates the possible footprint of a BGA. Given with the conventional method and materials required to produce a BGA device, the direction of miniaturized and downsized version of BGA became challenging.

Through realization of a specialized design of packaging and method of assembly, a package

design solution is discussed in this paper to provide a miniaturization with higher pin count capability by minimizing the RDL interconnections and channels through embedding an electrically connected bonding pads on the backside of the silicon die. Through this system, a substrate that is conventionally used for the re-routing of signals from the silicon die is eliminated and replaced by conductive via and routed channels or traces that are incorporated in the at the die backside.

2. DESIGN METHODOLOGY

Realization of the proposed design is composed of the silicon dies with top and bottom active sections that will be connected by a conductive via as shown in Fig. 2. The bottom active portion is embedded with a system such as nano-scaled transistor, resistor, capacitor, and active elements that are connected to a bond pad. The topside active portion is fabricated with routing and electrical channels that is linked to the bottom active system. A second silicon die is attached and wirebonded to the topside active portion to connect the bond pads to the routed interconnects.

The application of the proposed design eliminates the use of substrate or leadframe to transfer the signal to the designated I/O location. By removing the application of substrate in the direct material structure, the dimension is expected to lessen by 20 to 40 % from its designed size.

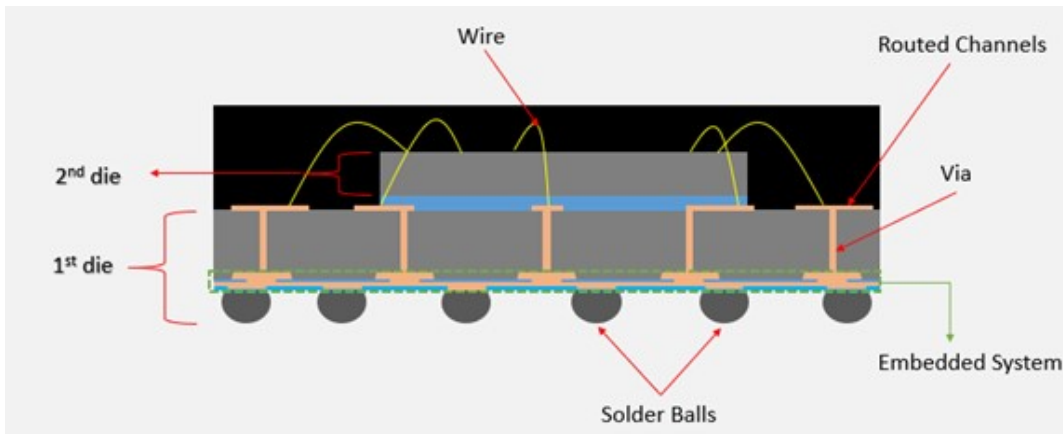


Fig. 2. Package with embedded routed channel

2.1 Silicon Die with Embedded Routed Channel

A silicon die is augmented to produce a routed channel through repeated cycle of masking and metal deposition process as depicted in Fig. 3. The fabrication of the routed channel on the surface of the silicon are produced from plating the bare silicon with a conductive material and etching the unnecessary portions of the plated metal to create a definite pattern of routed channels. Material such as Nickel-Palladium-Gold or Silver is recommended as plating material since it produce good intermetallic to semiconductor wire. In addition, immersion and selective plating process are alternative method in incorporating the metallic layers to the outer surface of the silicon die.

The routed channel is connected to the bond pad using a conductive via that will be drilled and filled with a conductive material. A single routed channel is designated to a single or multiple bond pad at the bottom of silicon die. A cross-sectional view of the silicon die is represented in Fig. 4. The routed channel is electrically connected to the bond pad at the opposite end of the conductive via.

The RDL is fabricated from the die system which carry the signal from the bond pad to the routed bonding pads. The bonding pad is connected either from the bottom circuitry (die system) or to the routed channel. The routed bond pad is where a solder will be attached to connect the unit to the external printed circuit board (PCB).

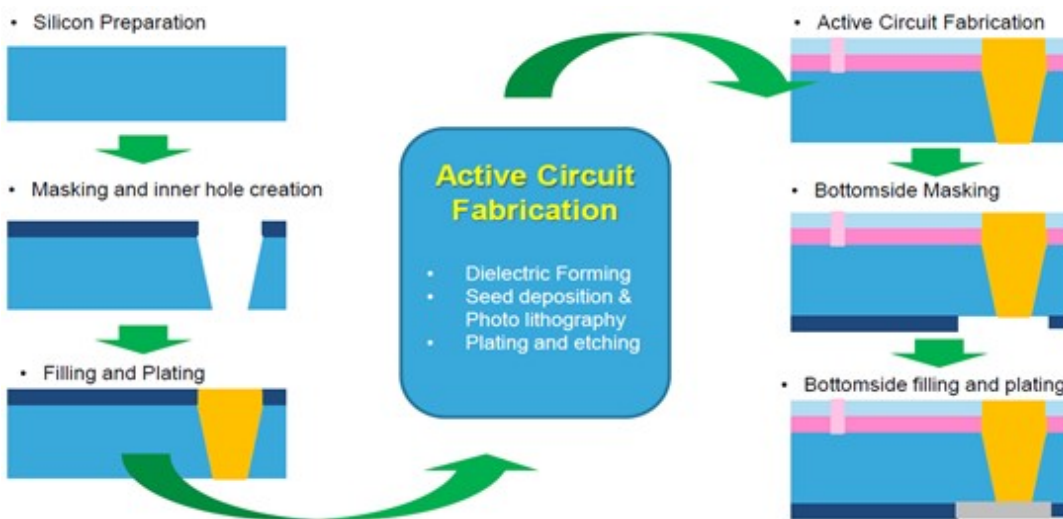


Fig. 3. Method of fabrication a silicon die

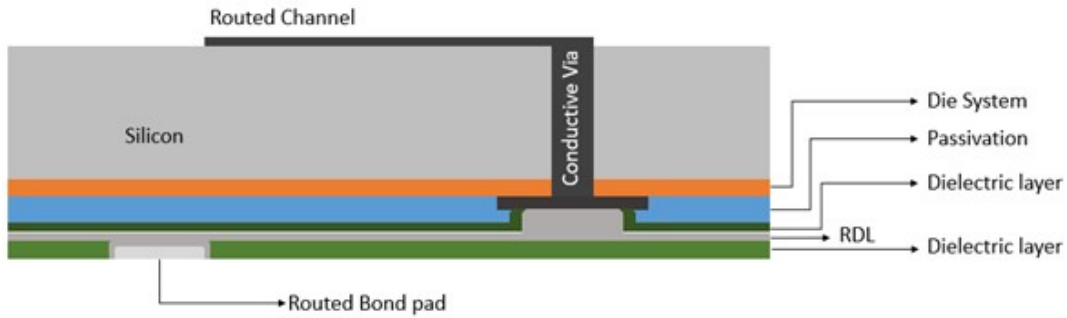


Fig. 4. Silicon die description

In Fabricating a routed bond pad, a dielectric layer is incorporated to the passivation layer of the silicon die to isolate the RDL electrically from die system. On the other hand, a second dielectric layer is used to insulate the RDL to the PCB. This layer protects and eliminates electrical shorting between interfaces.

2.2 Routed Bond Pad Design

The design of routed channels for silicon die 1 and 2 is shared in Fig. 5. Fig. 5A shows the array of I/O that will attach the unit to the PCB. Fig. 5B gives the routed channel design in topside view. Individual I/O is connected to a routed channel.

The second silicon die is attached on the surface using a non-conductive material. A die attach film (DAF) or non-conductive glue material is

recommended to isolate the second silicon die from the active routed channels. A semiconductor wire would attach the bond pad of the second silicon die to the routed channels.

2.3 Assembly Process

Assembly methodology of the design is shown in Fig. 6. The silicon die with embedded routing channel is picked from the wafer tape and transferred to a carrier material using “flip-chip” die attach machine. the carrier is composed of thermo-compression tape which is attached to a metal stiffener that will hold the units during its assembly. A second die bonding will be performed using standard die attach process to attach the second die on the topside section of the first silicon die. The bond pad from the second silicon die is attach to the routed channel using wire bonding process.

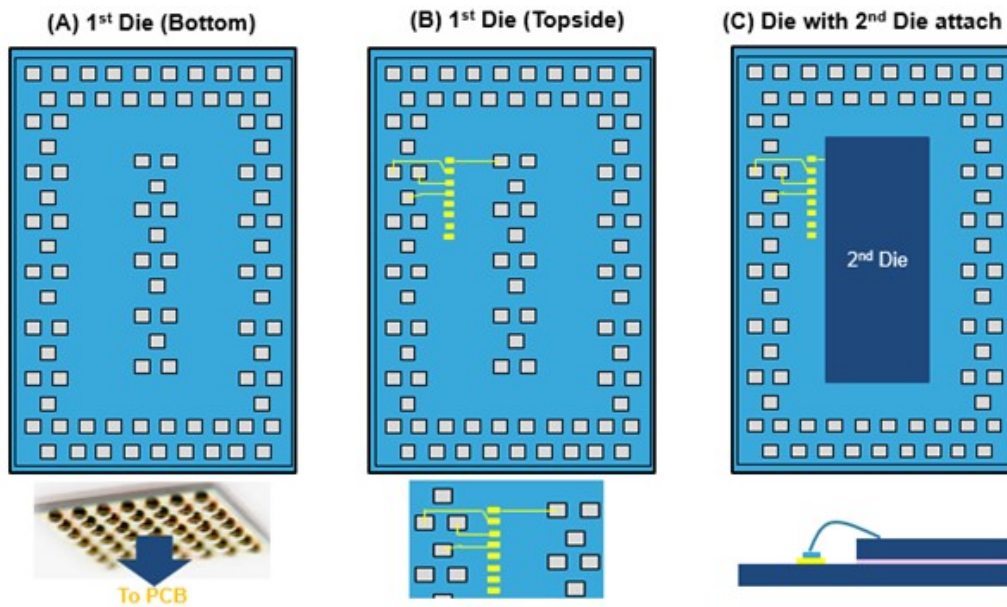


Fig. 5. Layout

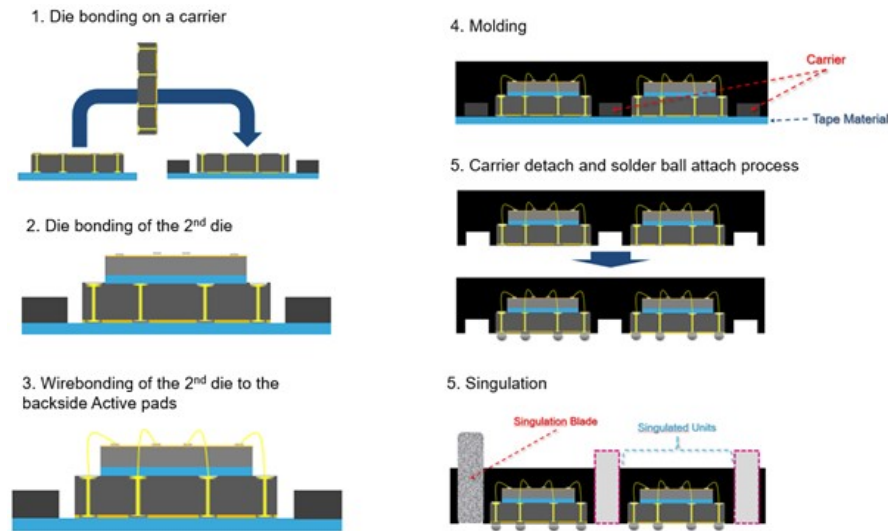


Fig. 6. Assembly process

Molding process is performed to encapsulate the units and carrier using epoxy molding compound. After the molded units is cured, the carrier (stiffener and tape) will be removed then solder balls will be attached to the solder mask opening of the unit. singulation process will be done after the stiffener is removed to separate the molded unit into individual units. Important to note that generally, process flow varies with the product and the technology [5-8].

3. CONCLUSION AND RECOMMENDATIONS

An augmented semiconductor package design was presented for high-density I/O capability. The limitations from the standard design is eliminated through the new design and the specialized fabrication process of the device. Ultimately, the package design solution would address the demanding high-density I/O requirement of complex designs.

Though the paper focused on the said condition, continuous process and design improvement is imperative to foster and sustain high quality performance of semiconductor products and its assembly manufacturing. Prototypes are helpful for future works to validate the effectiveness of the new package design.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
2. Sumagpang Jr A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMPE Technical Symposium, Philippines; 2012.
3. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008;1-11.
4. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
5. Coombs C, Holden H. Printed circuits handbook. 7th ed., McGraw-Hill Education, USA; 2016.

6. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; 2007.
7. Nenni D, McLellan P. Fables: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
8. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; 2004.

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