Journal of Intelligent Learning Systems and Applications, 2010, 2: 36-42
doi:10.4236/jilsa.2010.21005 Published Online February 2010 (http://www.SciRP.org/journal/jilsa)

Synthesis of Nonlinear Control of Switching Topologies of Buck-Boost Converter Using Fuzzy Logic on Field Programmable Gate Array (FPGA)

Johnson A. Asumadu, Vaidhyanathan Jagannathan, Arkhom Chachavalnanont

Electrical and Computer Engineering, Western Michigan University, Kalamazoo, USA.
Email: johnson.asumadu@wmich.edu

Received September 25th, 2009; accepted January 11th, 2010.

ABSTRACT

An intelligent fuzzy logic inference pipeline for the control of a dc-dc buck-boost converter was designed and built using a semi-custom VLSI chip. The fuzzy linguistics describing the switching topologies of the converter was mapped into a look-up table that was synthesized into a set of Boolean equations. A VLSI chip–a field programmable gate array (FPGA) was used to implement the Boolean equations. Features include the size of RAM chip independent of number of rules in the knowledge base, on-chip fuzzification and defuzzification, faster response with speeds over giga fuzzy logic inferences per sec (FLIPS), and an inexpensive VLSI chip. The key application areas are: 1) *on-chip integrated controllers; and* 2) *on-chip co-integration for entire system of sensors, circuits, controllers, and detectors for building complete instrument systems.*

Keywords: *Multi-Fuzzy Logic Controller* (*MFLC*), *Field Programmable Gate Array* (*FPGA*), *Buck-Boost Converter, Boolean Look-Up Table, Co-Integration*

1. Introduction

The design of control laws for power converters and inverters has been based mainly on linear control theory. However, most power electronics switching topologies have variable structures which are non-linear, characterized by discontinuities, and are therefore more difficult to model. The three most popular control methods used are state-space averaging technique [1], variable structure control (VSC) [2], and sliding mode control [3]. The state-space technique may lead to instability, the VSC control has hysteresis as drawback, and the sliding-mode control is very complicated. The implementation of the above-mentioned control laws are complicated, high cost and almost not practical.

Fuzzy logic controllers (FLCs) are very suitable for variable structures but current applications of FLCs use software for implementation. However, hardware implementation will be cheaper and faster. The proposed method combines hybrid linguistic models used in FLCs and computational paradigms of Boolean algebra. The knowledge base of the converter switching topologies is used to form a look-up table which is described by Boolean equations which are easily implemented using FPGA. Results showed that the size of the FPGA is independent of the number inference rules in the knowledge base, speeds in giga FLIPS are achieved because it is hardware based, and very fast control response.

2. Proposed Method

2.1 Single-Input-Single-Output (SISO) Fuzzy Controller

Consider the generalized buck-boost converter shown in Figure 1. This is a single-input-single-output (SISO) system. The input variable is the capacitor voltage (v_C) and the output variable is the duty ratio D. It can be shown that the average model has the following equations:

$$\frac{di_L(t)}{dt} = \frac{(1-D)v_C(t)}{L} + \frac{DE}{L} \quad (1)$$

$$\frac{dv_C(t)}{dt} = \frac{(1-D)i_L(t)}{C} - \frac{v_C(t)}{CR} \quad (2)$$

The membership functions for v_C and D are shown in Figure 2. The SISO system of Figure 1 has a single fuzzy input V (v_C) and a single fuzzy output D.

The fuzzy membership sets V and D are represented by five linguistic qualifiers L (low), ML (medium low), OK (okay), MH (medium high), and H (high). Hence there

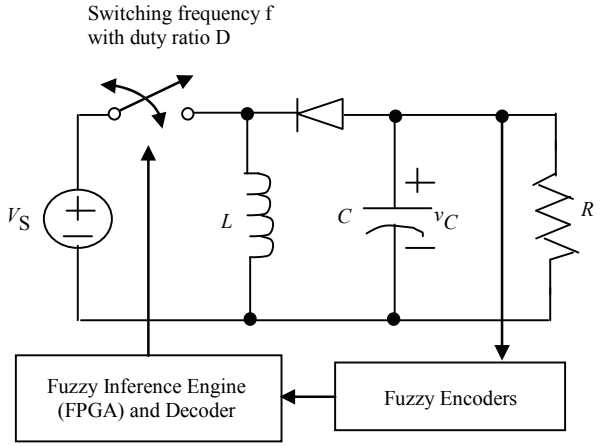


Figure 1. Buck-boost switching converter with a fuzzy controller

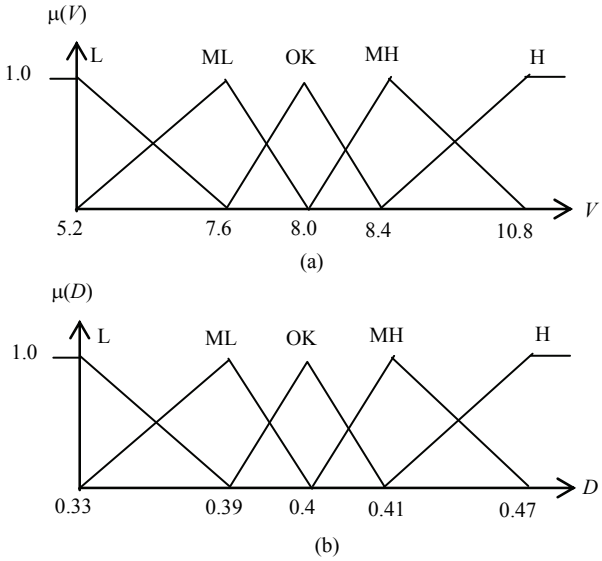


Figure 2. Membership functions for (a) voltage and (b) duty ratio

are 5x5=25 possible combinations that can generate 25 possible rules. However, the following 5 rules are sufficient to describe the membership values of Figure 2.

RULE 1: IF *V* is *H*, THEN *D* is *L*
RULE 2: IF *V* is *MH*, THEN *D* is *ML*
RULE 3: IF *V* is *OK*, THEN *D* is *OK* (3)
RULE 4: IF *V* is *ML*, THEN *D* is *MH*
RULE 5: IF *V* is *L*, THEN *D* is *H*

2.2 Logic Synthesis of Fuzzy Controllers

Consider a SISO fuzzy controller with input universe of discourse A^1 and output universe of discourse B^1. Manzoul [4] showed that the number of unique fuzzy inputs (ufi) is equal to the dimension of the input universe of discourse. That is:

$$\text{ufi}=\dim[A^1]=q_1 \quad (4)$$

In the fuzzification process, each input is mapped into only one value (one element) in the input universe of discourse and zero value to all other values (elements). The objective here is to use a look-up table. Therefore, the number of rows in the look-up table is equal q_1. It was also shown in [4] that the total least integer number of binary bits *X* for all the inputs is given by

$$X=\log_2\ q_1 \quad (5)$$

Each fuzzy input has only one output value and therefore the maximum number of distinct output values is also equal to q_1. In the defuzzification process only one element is selected in the output universe of discourse. It is therefore, easier and economical to use the defuzzified

outputs in the look-up table. If the there are p elements ($p \leq q_1$) in the output universe of discourse, the dimension of the output universe of discourse is given as

$$\dim[B^1]=p \quad (6)$$

The total least integer number of binary bits Y for all the outputs is given by

$$Y=\log_2 p \quad (7)$$

3. Buck-Boost Converter Fuzzy Controller

3.1 Fuzzy Controller

Consider a SISO controller to control the output voltage of the buck-boost converter of Figure 1. The input variable is the voltage and output variable is the duty ratio. The duty ratio maintains the voltage at a selected value. The ranges of capacitor voltage (v_C) and duty ratio D are (5.2 to 10.8) V and (0.33 to 0.47) respectively. The membership values are in the interval [0, 1], where 0 denotes no membership and 1 denotes full membership. Assume that

$$\text{im}[V^1]=\dim[D^1]=29 \quad (8)$$

From (5) the least number of binary bits to represent the input values is given as

$$X=\log_2 29=5$$

Similarly, using (6) the least number of binary bits to represent output values is given as

$$Y=\log_2 29=5$$

In Appendix I the 5 rules of (3) are expressed numerically. The fuzzy relation obtained is too big to be shown here because of the size (29x29 matrix). Table 1 of Appendix I shows the summary of the complete computations of the controller.

3.2 Look-Up Table

The look-up table representing the fuzzy controller is given in Table 2. The input universe of discourse has dimension of 29 and the output universe has dimension of 29. The look-up can be described by 7-variable Boolean equations. That is,

$$\begin{aligned}
f0&=\sum (5,6,8,9,10,12,16,17,1923,26,27,28)\\
f1&=\sum (2,4,5,7,8,10,11,14,17,18,21,24,27)\\
f2&=\sum (2,3,5,6,8,9,14,15,16,21,22,24, 25,27,28,29)\\
f3&=\sum (1,5,6,7,14,16,17,18,19,20,24,25,26) \quad (9)\\
f4&=\sum (1,2,3,4,14,24,25,26,27,28,29)\\
f5&=\sum (1,2,3,4,5,6,7,8,9,10,11,12,13,16,17,18,19, 20, 21, 22, 23)\\
f6&=\sum (1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)
\end{aligned}$$

Table 1. Summary of the controller computations

Input Voltage	Fuzzified Input	Fuzzy Output	Output Duty Ratio (X)
0.0 - 5.20	1.0, 0.0, 0.0, ., ., ., 0.0	*0,0,.08,.16,.25,.33,.41,.5,.58,.66,.75,.83,.91,1.0	120
5.21 - 5.40	0.0, 1.0, 0.0, ., ., ., 0.0	*,.08,.08,.08,.16,.25,.33,.41,.5,.58,.66,.75,.83,.91,.91	118
5.41 - 5.60	0.0, ., ., 1.0, ., ., ., 0.0	*,.16,.16,.16,.16,.25,.33,.41,.5,.58,.66,.75,.83,.83,.83	116
5.61 - 5.80	0.0, ., ., 1.0, ., ., ., 0.0	*,.25,.25, ,.25, ,.25, ,.25,.33,.41,.58,.66,.75,.75,.75,.75	114
5.81 - 6.00	0.0, ., ., 1.0, ., ., ., 0.0	*,.33,.33,.33,.33,.33,.33,.41,.5,.58,.66,.66,.66,.66,.66	111
6.01 - 6.20	0.0, ., ., 1.0, ., ., ., 0.0	*,.41,.41,.41,.41,.41,.41,.41,.5,.58,.58,.58,.58,.58,.58	109
6.21 - 6.40	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5	106
6.41 - 6.60	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.58,.58,.58,.58,.58,.58,.5,.41,.41,.41,.41,.41,.41,.41	103
6.61 - 6.80	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.66,.66,.66,.66,.66,.58,.5,.41,.33,.33,.33,.33,.33	101
6.81 - 7.00	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.75,.75,.75,.75,.66,.58,.5,.41,.33,.25, ,.25, ,.25, ,.25	99
7.01 - 7.20	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.83,.83,.83,.75,.66,.58,.5,.41,.33,.25,.16,.16,.16	98
7.21 - 7.40	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,.91,.91,.83,.75,.66,.58,.5,.41,.33,.25,.16,.08,.08	97
7.41 - 7.60	0.0, ., ., 1.0, ., ., ., 0.0	*,.5,1.0,.91,.83,.75,.66,.58,.5,.41,.33,.25,.16,.08,.0	96
7.61 - 7.80	0.0, ., ., 1.0, ., ., ., 0.0	**,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.41,.33,.25,.16,.08,0.0	94
7.81 - 8.00	0.0, ., ., 1.0, ., ., ., 0.0	**,.5,1.0,.5,**	70
8.01 - 8.20	0.0, ., ., 1.0, ., ., ., 0.0	0,.08,.16,.25,.33,.41,.5,.5,.5,.5,.5,.5,.5,.5,.5,**	45
8.21 - 8.40	0.0, ., ., 1.0, ., ., ., 0.0	0,.08,.16,.25,.33,.41,.5,.58,.66,.75,.83,.91,1.0,.5,*	43
8.41 - 8.60	0.0, ., ., 1.0, ., ., ., 0.0	.08,.08,.16,.25,.33,.41,.5,.58,.66,.75,.83,.91,.91,.5,*	42
8.61 - 8.80	0.0, ., ., 1.0, ., ., ., 0.0	.16,.16,.16,.25,.33,.41,.58,.66,.75,.75,.75,.75,.5,*	41
8.81 - 9.00	0.0, ., ., 1.0, ., ., ., 0.0	.25, ,.25, ,.25, ,.25,.33,.41,.58,.66,.75,.75,.75,.75,.5,*	40
9.01 - 9.20	0.0, ., ., 1.0, ., ., ., 0.0	.33,.33,.33,.33,.33,.41,.5,.58,.66,.66,.66,.66,.66,.5,*	38
9.21 - 9.40	0.0, ., ., 1.0, ., ., ., 0.0	.41,.41,.41,.41,.41,.41,.5,.58,.58,.58,.58,.58,.58,.5,*	36
9.41 - 9.60	0.0, ., ., 1.0, ., ., ., 0.0	.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,.5,*	33
9.61 - 9.80	0.0, ., ., 1.0, ., ., ., 0.0	.58,.58,.58,.58,.58,.58,.5,.41,.41,.41,.41,.41,.41,.41,*	30
9.81 - 10.00	0.0, ., ., 1.0, ., ., ., 0.0	.66,.66,.66,.66,.66,.66,.58,.5,.41,.33,.33,.33,.33,.33,.33,*	28
10.01 - 10.20	0.0, ., ., 1.0, ., ., ., 0.0	.75,.75,.75,.75,.66,.58,.5,.41,.33,.25, ,.25, ,.25, ,.25,.25,*	25
10.21 - 10.40	0.0, ., ., 1.0, 0.0, 0.0	.83,.83,.83,.75,.66,.58,.5,.41,.33,.25,.16,.16,.16,.16,*	23
10.41 - 10.60	0.0, ., ., 0.0, 1.0, 0.0	.91,.91,.83,.75,.66,.58,.5,.41,.33,.25,.16,.08,.08,.08,*	21
10.61 - 10.8	0.0, ., ., 0.0, 0.0, 1.0	1.0,.91,.83,.75,.66,.58,.5,.41,.33,.25,.16,.08,.0,.0,*	20

NOTE: *=0,0,0,0,0,0,0,0,0,0,0,0,0,0,0 **=0,0,0,0,0,0,0,0,0,0,0,0,0,0

Duty ratio D=-0.0011051*X+0.4

Table 2. Look-up table for fuzzy controller

INPUT						OUTPUT							
#	BINARY					#	BINARY						
	y_4	y_3	y_2	y_1	y_0		f_6	f_5	f_4	f_3	f_2	f_1	f_0
1	0	0	0	0	1	120	1	1	1	1	0	0	0
2	0	0	0	1	0	118	1	1	1	0	1	1	0
3	0	0	0	1	1	116	1	1	1	0	1	0	0
4	0	0	1	0	0	114	1	1	1	0	0	1	0
5	0	0	1	0	1	111	1	1	0	1	1	1	1
6	0	0	1	1	0	109	1	1	0	1	1	0	1
7	0	0	1	1	1	106	1	1	0	1	0	1	0
8	0	1	0	0	0	103	1	1	0	0	1	1	1
9	0	1	0	0	1	101	1	1	0	0	1	0	1
10	0	1	0	1	0	99	1	1	0	0	0	1	1
11	0	1	0	1	1	98	1	1	0	0	0	1	0
12	0	1	1	0	0	97	1	1	0	0	0	0	1
13	0	1	1	0	1	96	1	1	0	0	0	0	0
14	0	1	1	1	0	94	1	0	1	1	1	1	0
15	0	1	1	1	1	70	1	0	0	0	1	1	0
16	1	0	0	0	0	45	0	1	0	1	1	0	1
17	1	0	0	0	1	43	0	1	0	1	0	1	1
18	1	0	0	1	0	42	0	1	0	1	0	1	0
19	1	0	0	1	1	41	0	1	0	1	0	0	1
20	1	0	1	0	0	40	0	1	0	1	0	0	0
21	1	0	1	0	1	38	0	1	0	0	1	1	0
22	1	0	1	1	0	36	0	1	0	0	1	0	0
23	1	0	1	1	1	33	0	1	0	0	0	0	1
24	1	1	0	0	0	30	0	0	1	1	1	1	0
25	1	1	0	0	1	28	0	0	1	1	1	0	0
26	1	1	0	1	0	25	0	0	1	1	0	0	1
27	1	1	0	1	1	23	0	0	1	0	1	1	1
28	1	1	1	0	0	21	0	0	1	0	1	0	1
29	1	1	1	0	1	20	0	0	1	0	1	0	0

3.3 Control Instrument Implementation

3.3.1 FPGA Implementation

The FPGA configuration is implemented by using Xilinx's X95 (XC9536-10-PC44 CPLD) and XS40 (XC40 05XL FPGA) boards. Both boards come with 8051 microcontroller with 12 MHz speed. The Xilinx's development system is used to implement the Boolean equations, which also represents the fuzzy controller. Figure 3 shows the semi-custom VLSI chip of the FPGA functional block diagram.

3.3.2 Instrument

Figure 4 shows the diagram of the fuzzy logic controller chip pin outs and output waveforms. The binary inputs of the controller $y_0, y_1, \ldots, y_4$ are the encoded fuzzified crisp output voltage v_C of the dc-dc converter. The binary outputs of the controller $f_0, f_1, \ldots, f_6$ are defuzzified to provide the variable duty ratio D.

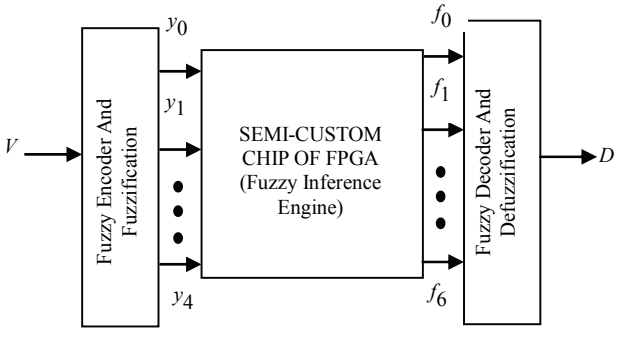
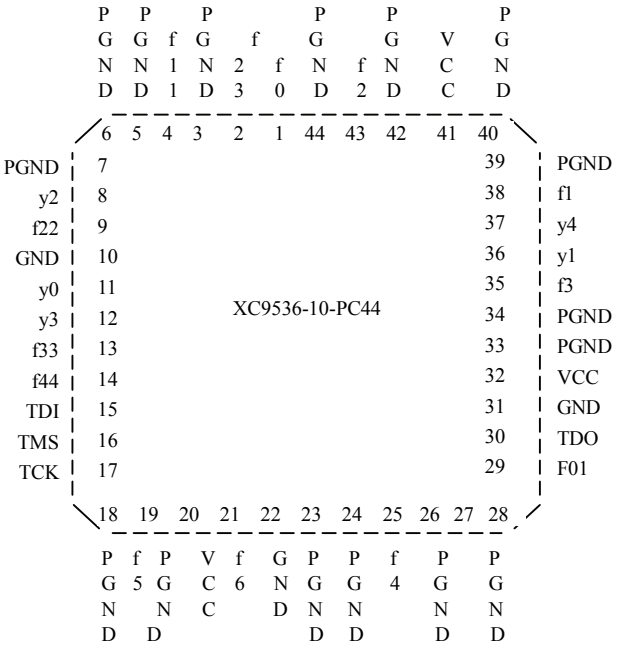


Figure 3. Semi-custom VLSI fuzzy controller chip

3.3.3 On-Chip Cointegration

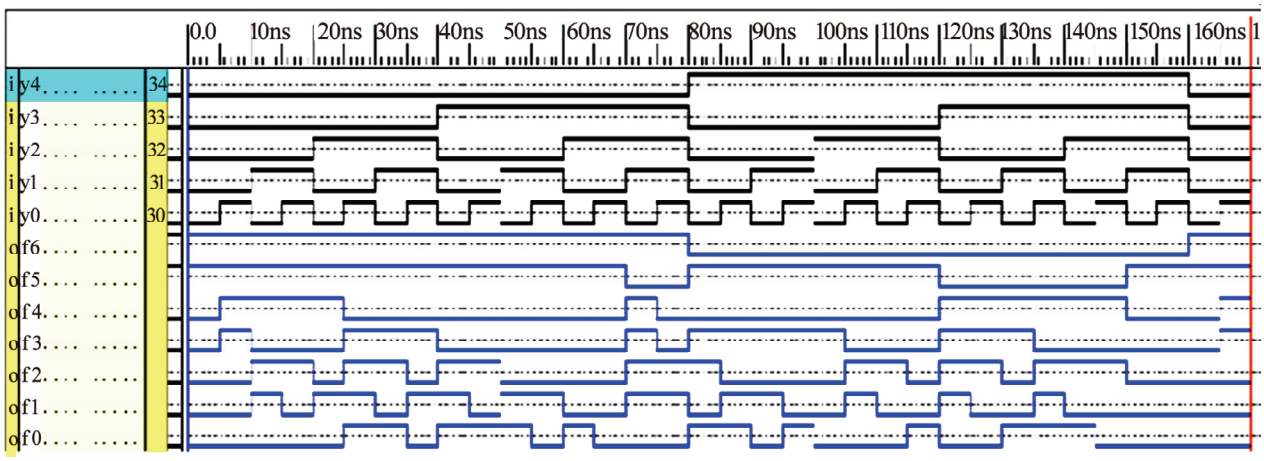
Microsystems technology has made inroads in instrumentation and measurement (I&M) applications. The fuzzy logic FPGA controller chip can be fabricated to have compact size. The FLC chip of this paper provides an interesting fabrication technique that has been identified in I&M applications: cointergration of control/sensors/detectors and circuits for building complete instrument systems.

The on-chip controller mentioned in the paper uses a compact FPGA chip, which can be fabricated as part of an integrated system of sensors, circuits, controllers, and detectors squeezed onto nanometer wafer. Such microchips can be used in a variety of applications in different environments and requirements. Besides mass volume production of these microchips, there are other advantages such as cheaper parts and assembly of instruments, better functionality, lower mass and size, speed of control, lower cost, and higher efficiency. Some companies are now using multi fuzzy logic controller-based (MFLC) chips in some of their new dryers, dishwashers, and washing machines.



Legend : PGND = Tie pin to GND for additional ground path or leave unconnected
VCC = Dedicated Power Pin
GND = Dedicated Ground Pin
TDI = Test Data In, JTAG pin
TDO = Test Data Out, JTAG pin
TCK = Test Clock, JTAG pin
TMS = Test Mode Select, JTAG pin
PROHIBITED = User reserved pin

(a)



(b)

Figure 4. (a) FPGA pin out; (b) input and output waveforms of FLC chip

4. Results

The output voltage of Figure 1 is regulated at about 8.0 V through a feedback loop using the fuzzy controller on FPGA chip for adjusting the duty ratio D. The input voltage V_s=12 V and the circuit parameters are L=100 μH, C=330 μF. The steady-state voltage is about 8.0 V when the load R is changed from 10 Ω to 5 Ω. Figure 5 shows the test results of a fuzzy controller chip.

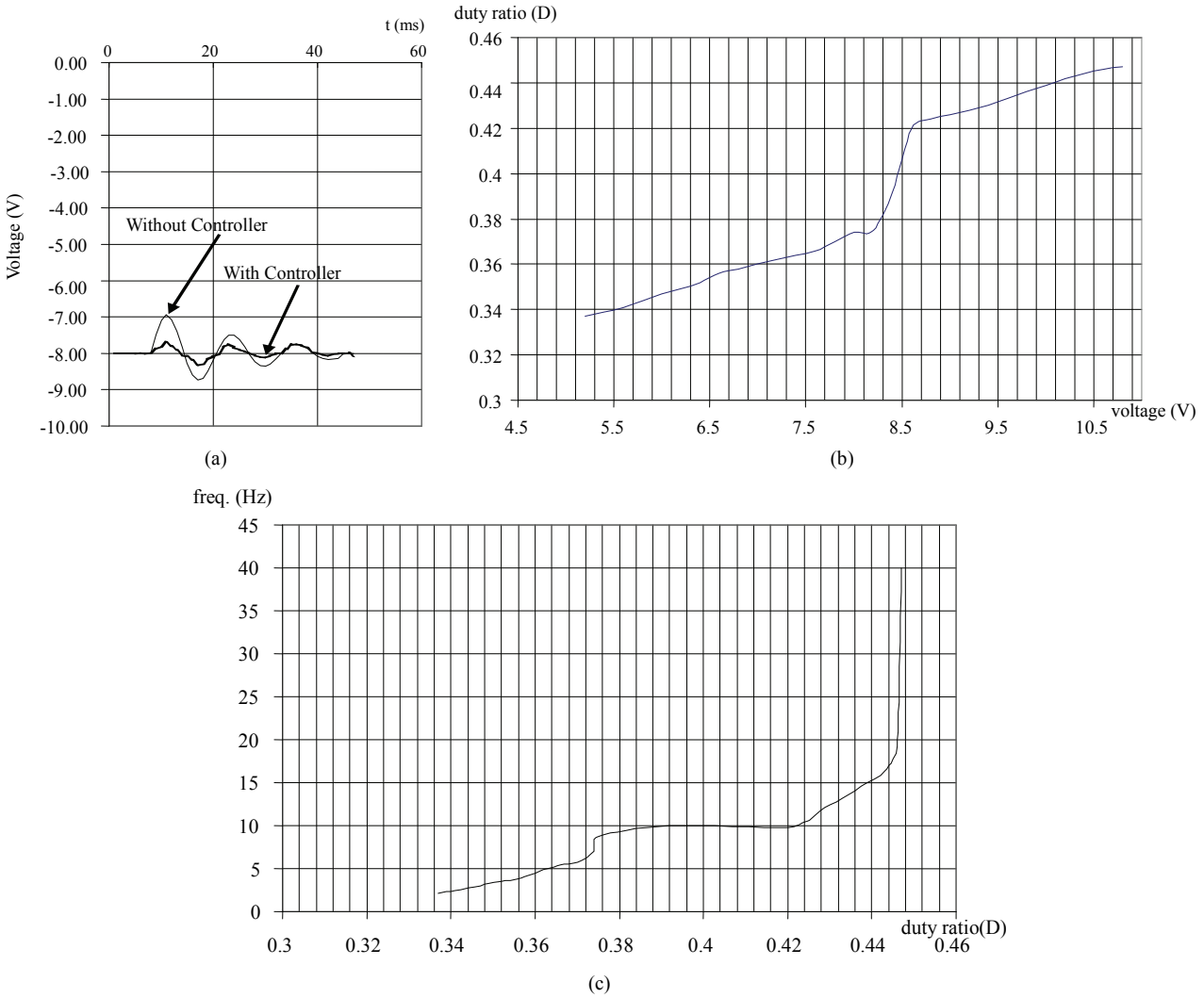


Figure 5. (a) Buck-boost converter results; (b) graph between voltage & duty; (c) relationship of frequency & duty ratio

Figure 5(a) shows the effect on the output voltage when changing the load resistance. Figure 5 shows that the output voltage $v_c(t)$ can respond instantaneously to changes in the duty ratio D. The hardware implementation is cheaper and faster than using software.

5. Conclusions

The fuzzy controller implemented on an FPGA was used to control a dc-dc buck-boost switching converter. The size of the semi-custom VLSI was independent of the number of rules in the knowledge base and therefore no memory space was required to store the large of rules. The important aspect of the controller is that it was hardware-based and consequently speeds over giga FLIPS can be achieved. The on-chip controller is a compact FPGA which may be integrated with sensors and circuits to provide a complete co-integration system.

REFERENCES

[1] R. Erickson, S. Cuk, and R. D. Middlebrook, "Large-signal modeling and analysis of switching regulators," IEEE PESC, pp. 240–250, 1982.

[2] W. Gao and J. C. Hung, "Variable structure control of non-linear systems," IEEE Transactions on Industrial Electronics, Vol. 40, No. 1, pp. 45–55, February 1993.

[3] H. Sira-Ramirez and M. Rios Bolivar, "Sliding-mode control of DC-DC power converters via extended-linearization," IEEE Transactions on Circuits and Systems I, Vol. 41, No. 10, 1994.

[4] M. A. Manzoul, "Fuzzy controllers on semi-custom VLSI chips," Fuzzy Control Systems, CRC Press, Inc., Boca Raton, Florida, pp. 551–560, 1994.

APPENDIX I

The 5 Rules of Equation 3 Expressed Numerically

RULE 1:
IF
[0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.08,0.16,0.25,0.33,0.41,0.5,0.58,0.66,0.75,0.83,0.91,1.0]
THEN
[1.0,0.91,0.83,0.75,0.66,0.58,0.5,0.41,0.33,0.25,0.16,0.08, 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0]

RULE 2:
IF
[0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.5,1.0,0.91,0.83,0.75,0.66,0.58,0.5,0.41,0.33,0.25,0.16,0.08,0]
THEN
[0.08,0.16,0.25,0.33,0.41,0.5,0.58,0.66,0.75,0.83,0.91,1.0,0.5, 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0]

RULE 3:
IF
[0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.5,1.0,0.50,0,0,0,0,0,0,0,0,0,0,0,0,0]
THEN
[0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.5,1.0,0.50,0,0,0,0,0,0,0,0,0,0,0,0,0]

RULE 4:
IF [0.08,0.16,0.25,0.33,0.41,0.5,0.58,0.66,0.75,0.83,0.91,1.0,0.5, 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0]
THEN [0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.5,1.0,0.91,0.83,0.75,0.66,0.58,0.5,0.41,0.33,0.25,0.16,0.08,0]

RULE 5:
IF [1.0,0.91,0.83,0.75,0.66,0.58,0.5,0.41,0.33,0.25,0.16,0.08, 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0]
THEN [0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0.08,0.16,0.25,0.33,0.41,0.5,0.58,0.66,0.75,0.83,0.91,1.0]